ABSTRACT OF THE DISCLOSURE

An input circuit is coupled to a first bus to transfer a delayed transaction (DT) data having a transaction identifier to one of N buffers. The input circuit is dynamically configured according to a bus frequency. N is a positive integer. The one of the N buffers is associated with the transaction identifier. An output circuit is coupled to the buffers to transfer the DT data from the one of the N buffers to a second bus operating at the bus frequency. The output circuit is dynamically configured according to the bus frequency.